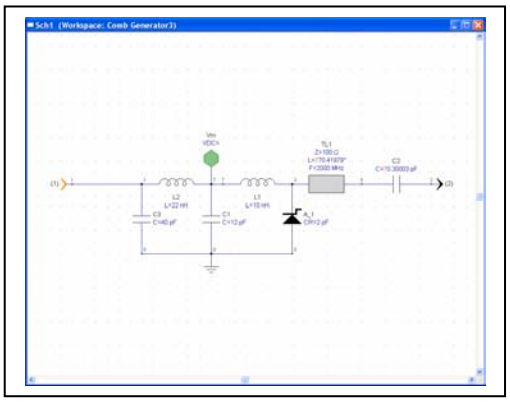
Eagleware App Note 22

Nonlinear Modeling of Step Recovery Diodes Using Verilog-A



Introduction

The Advanced Modeling Kit (AMK) in GENESYS contains an innovative Verilog-A compiler. This nonlinear modeling tool enables both the semiconductor modeling industry and design engineers to create and implement new complex linear and non-linear models that cover a wide range of behavioral characteristics.

Verilog-A Compiler

Based on the IEEE Verilog-A standard, extensive libraries of functions and an intuitive language help modelers and design engineers develop and deploy new functionality in minimum time. Illustrating the flexibility and utility available with the AMK, GENESYS offers VBIC, HiSIM, MEXTRAM and other models in Verilog-A source code and compiled models. Verilog-A source code is easier to read, requires less lines of code, and - after compilation - runs nearly as fast as a model written in C-code. The AMK does not limit the designer to pre-established models, although new models or features can be developed by using an existing model as a foundation. With the AMK you can develop models to describe and simulate the behavior of transistors, FETs, diodes, laser diodes, PIN receivers, non-linear magnetic devices and more.

The design procedure starts with a text editor. Either from scratch or from one of the many Verilog-A examples, a text file is developed that describes the terminal behavior of the device. In many cases the temperature and parasitic dependencies are also modeled and a table of parameters is established, enabling users of the model to enter additional parametric characteristics. Once the text file is complete, the file is stored in the "My Models" directory with a va name extension. When GENESYS is started, any va files are automatically compiled and linked into the GENESYS engine. The new model can then be used in the same manner as any other model in the design environment.

Modeling a Step Recovery Diode

A model of a step recovery diode was implemented to illustrate the use of the AMK. The step recovery diode (SRD), or "snap diode," has an unusual operating characteristic whenever forward biased charge is stored in the depletion region. During the reverse cycle, when the stored charge is removed, the conduction abruptly halts. This abrupt halt explains the diode's name: "snap diode". The abrupt current change is utilized to produce sampling devices and frequency multipliers.

To develop the SRD model we start with the Verilog-A description of a SPICE-like non-linear diode. From this starting point we add parameters describing the diode's capacitance, lead inductance, reverse recovery time, series resistance and other diode parameters. Next, the section that describes the capacitance/charge characteristics is modified to mimic the charge characteristics vs. voltage of a step recovery diode (See Appendix). When completed, the file is saved in the 'My Models' directory and when GENESYS is next started it automatically checks for new file revisions, compiles and loads the model for use. The only additional feature to add is a custom symbol, if desired. The process completed, the SRD model is now available for simulation via the parts library manager or pull-down menus.

Comb Generator

Figure 1 shows the design of a comb generator using the AMK-created model. Simulation was completed with GENESYS HARBEC using 30 harmonics with an input frequency of 200 MHz and power of +26 dBm.

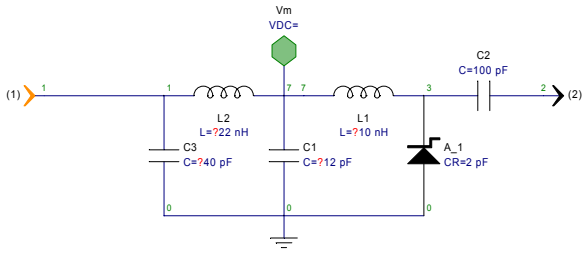


Figure 1

The topology in Figure 1 uses the typical series inductance L1 to provide the impulse shape. As stated previously, when the diode current abruptly shuts off as a result of the forward bias charge being depleted, a voltage spike is generated as a result of L di/dt. The pulse width is usually designed either to produce a rich set of harmonics—such as in the comb generator example for broadband mixing, Figure 1, or shaped to enhance a particular multiple of the input frequency as illustrated in the X10 multiplier in Figure 5. The additional lumped components, L2 and C3, provide a match to the source impedance at the driven frequency[1].

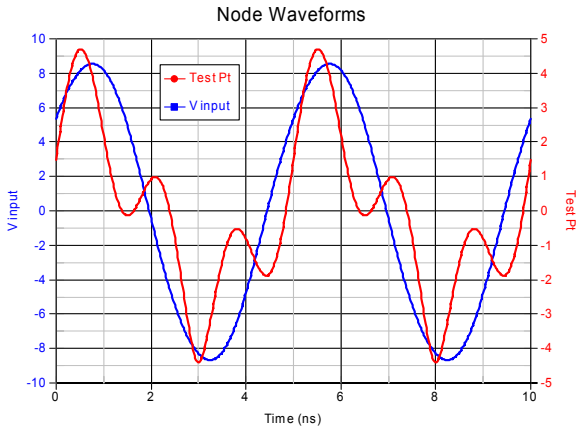


Figure 2

Figure 2 notes the voltage waveforms at the input of the comb generator and at the junction of L1, L2, and C1. Note that the impulse has not been totally filtered at this point. Figure 3 shows the impulse generated into the 50 ohm load. Pulse width is approximately 180 ps.

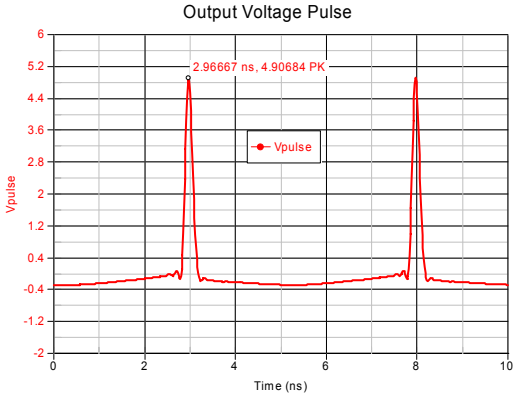


Figure 3

By varying parameters such as junction capacitance, reverse recovery time, and parasitic inductance, different pulse shapes optimized for the task required can be manipulated based upon manufacturer's data sheets. Figure 4 illustrates a non-optimized comb. Note that power drops by only 10db up to the 15th harmonic.

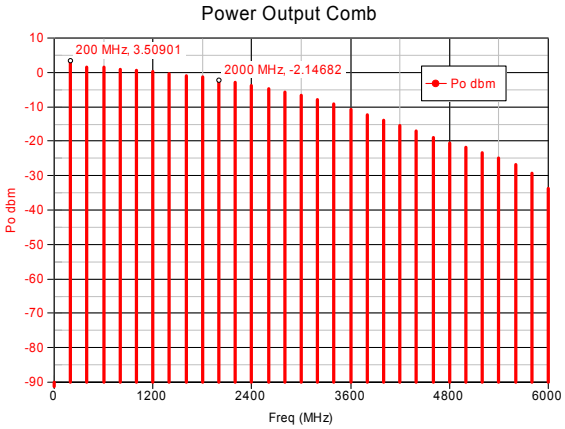


Figure 4

[1] Hewlett Packard Application Note 920

10X Multiplier Example

To further illustrate the potential gain in using the AMK, a 10X multiplier was simulated. Starting with the basic comb generator design, a frequency selective output resonator, consisting of a length of transmission line and coupling capacitor, was added. Figure 5 illustrates the final schematic configuration.

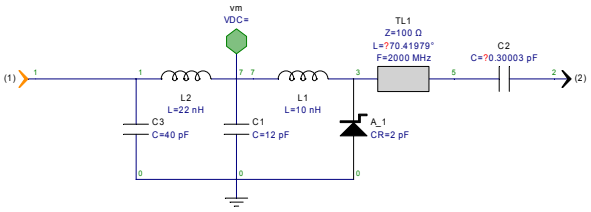


Figure 5

Once a final design is realized, the Advanced T/LINE feature in GENESYS converts the transmission topologies into their final form (i.e. microstrip) without further effort by the designer. The node voltages for the completed multiplier are shown in Figures 6 and 7.

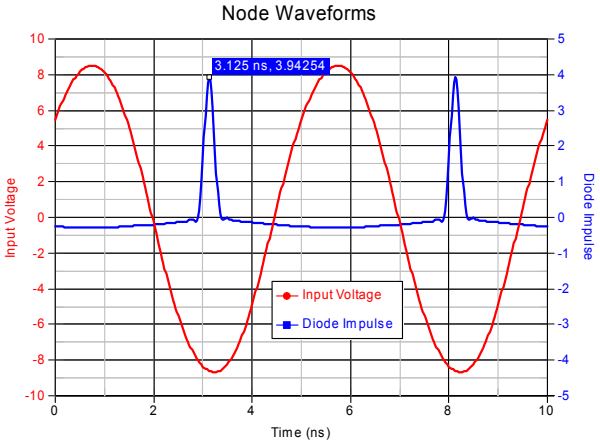


Figure 6

Figure 6 shows the input waveform and that of the impulse at the diode/transmission line node.

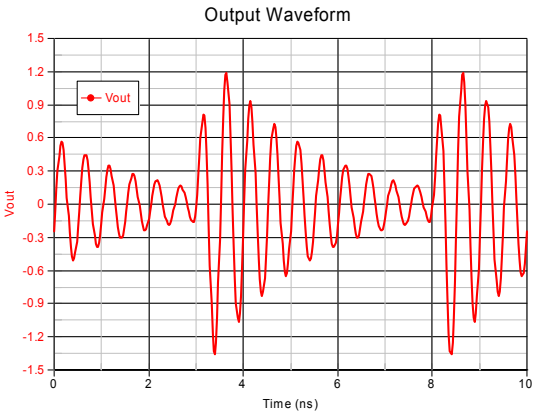


Figure 7

Figure 7 illustrates the ringing waveform at the 50 load. The electrical length, line impedance, and coupling capacitor all affect the shape and frequency response of the final signal. The goal of varying these component values is to maximize the power available in Nth comb.[2] Finally, Figure 8 provides a look at the output spectrum centered around 2 GHz (X10 of input frequency). Typically, additional filtering is required if the multiplier has more stringent harmonic content requirements. This may be implemented with lumped or distributed filters that are dictated by the operating frequency. Fortunately GENESYS offers synthesis tools that cover the range with M/FILTER and FILTER.

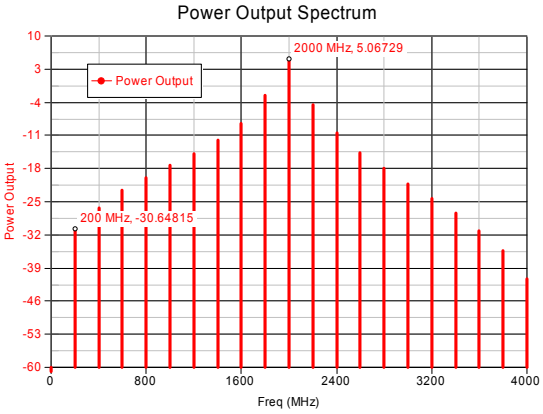


Figure 8

[2] Hewlett Packard Application Note 918

Appendix

```
/*
 Eagleware 2003 Bill Clausen
Implementation of a step recovery diode as defined by Zhang and Raissanen in
"A New Model of Step Recovery Diode for CAD" MTT-S 1995 p 1459-1462
*/
`include "constants.vams"
`include "disciplines.vams"

`define SPICE_GMIN 1.0e-12
`define LARGE_REAL 1.0e99
`define DEFAULT_TNOM 27

module diode_srd(anode,cathode);

   // %%DEVICE_CLASS=DIODE%%

    inout anode, cathode;
    electrical anode, cathode, internal;

    parameter real Area = 1.0 from (0:inf];  //Area scaling factor
    parameter real Is = 1e-14 from [0:inf];  //Saturation current [A]
    parameter real Tnom = `DEFAULT_TNOM from (-`P_CELSIUS0:inf); //Measurement temp[C]
    parameter real Rs = 0.0 from [0:inf];    //Ohmic res [Ohm]
    parameter real Rf = 0.1 from [0:inf];     // Forward biased resistance[Ohm]
    parameter real Tt = 0.0 from [0:inf];    //Transit time [s]
    parameter real Tau = 2e-9 from [0:inf];     // Reverse recovery time[s]
    parameter real Cr = 0.0 from [0:inf];    //Junction capacitance [F]
    parameter real Lpk = 1e-9 from [0:inf];      //Package Inductance [H]
    parameter real Cpk = 2e-12 from [0:inf];      // Package Capacitance[F]
    parameter real Vj = 1.0 exclude 0;              //Junction potential [V]
    parameter real N = 1.0 from [0:inf];     //Emission coef
    parameter real M = 0.5 from [0:inf];     //Grading coef
    parameter real Eg = 1.11 from (0:inf];   //Activation energy [eV]
    parameter real Xti = 3.0 from [0:inf];   //IS temp exp.
    parameter real Kf = 0.0;                 //Flicker noise coef
    parameter real Af = 1.0 from (0:inf);    //Flicker noise exponent
    parameter real Fc = 0.5 from [0:1];             //Forward bias junct parm
    parameter real Bv = 60.0 from [0:inf];   //Reverse breakdown voltage [v]
    parameter real Ibv = 0.001 from [0:inf];//Current at BV [A]

    real Vd, Id, Qd, Cf;
    real f1, f2, f3, Fcp;
    real Ibv_calc, Vth;
    real Is_temp, Vth_nom, T_nom, T;

    analog begin

      Vth = $vt;
       T = $temperature;

       f1 = (Vj/(1 - M))*(1 - pow((1 - Fc), 1 - M));
       f2 = pow((1 - Fc), (1 + M));
       f3 = 1 - Fc * (1 + M);
       Fcp = Fc * Vj;

         Cf = Tau/Rf;

       if (Ibv !=0)
           Ibv_calc = Ibv;
       else
           Ibv_calc = Is * Bv / Vth;

       Vd = V(anode, internal);

       // Temperature dependence
       T_nom = Tnom + `P_CELSIUS0;
       Vth_nom = $vt(T_nom);
       Is_temp = Is * pow(T/T_nom, Xti / N) * limexp(Eg / Vth_nom - Eg / Vth);
```

```
        // Intrinsic diode
        // BV is not adjusted to match Ibv if I(BV) <> Ibv
        if (Vd < 0) begin
            if (Vd < -Bv) // Past breakdown
                Id = -Area * Is_temp * (limexp(-(Bv + Vd) / Vth) + Bv / Vth);
            else if (Vd == -Bv) // At breakdown
                Id = -Area * Ibv_calc;
            else if (Vd <= -5 * N * Vth) // -Bv < Vd < -5 nKT/q
                Id = -Area * Is_temp + Vd * `SPICE_GMIN;
            else // -5 nKT/q <= Vd < 0
                Id = Area * Is_temp * (limexp(Vd / Vth) - 1) + Vd * `SPICE_GMIN;
         end
         else // Fwd bias:
             Id = Area * Is_temp * (limexp(Vd / (N * Vth)) - 1) + Vd * `SPICE_GMIN;

        // Capacitance (junction and diffusion)
        if (Vd <= 0)

           Qd = Cr*Vd;

           else if ((Vd > 0.0)&&(Vd < Fcp))
            Qd = (Cf-Cr/2*Fcp)*pow((Vd+(Cr*Fcp)/(Cf-Cr)),2)-(Cr*Cr*Fcp)/(2*(Cf-Cr));

           else
            Qd = Cf*Vd-(Cf-Cr)*Fcp/2;


        I(anode, internal) <+ Id;
        V(internal, cathode) <+ I(internal, cathode) * (Rs / Area) + Lpk*ddt(Id);
        I(anode, internal) <+ ddt(Qd);


    end

endmodule
```

References

Additional Sources of Information

1) "A Circuit Model of the Step Recovery Diode," K.L. Kotzebue, Proceedings of the IEEE, December, 1965, pg 2119-2120.
2) "Computer Aided Design of Step Recovery Diode Frequency Multipliers," Jian Zhang and Antti V. Raisanen, MTT, vol 44, No.12, December, 1996, pg 2612-2616.
3) "Shunt Harmonic Generation Using Step Recovery Diodes," Stephen Hamilton, Robert Hall, Microwave Journal, April 1967, pg 69-78.
4) "Pulse and Waveform Generation with Step Recovery Diodes," Hewlett Packard Application Note 918.
5) "Harmonic Generation Using Step Recovery Diodes and SRD Modules," Hewlett Packard Application Note 920.
6) "Ku-band Step Recovery Multipliers," Hewlett Packard Application Note 928.
7) "Comb Generator Simplifies Multiplier Design," Hewlett Packard Application Note 983.